UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,885	06/19/2003	Jonathan B. Ballagh	X-1408 US	5917

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EXAMINER
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ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/600,885	BALLAGH ET AL.
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>19 June 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-13</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-13</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>19 June 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>June 19, 2003</u>.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

1.   Claims 1-13 of the application have been examined.

Information Disclosure Statement

2.   Acknowledgment is made of the information disclosure statements filed on June

19, 2003 together with a list of patents. The patents have been considered.

Drawings

3.   The drawings submitted on June 19, 2003 are accepted.

Specification

4.   Page 7, Para 0028, Lines 2-3, "reconfigurable hardware platform 108" appears to

be incorrect, since the re-configurable hardware platform is numbered 110 in Fig. 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.

6.   The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

    1.   Determining the scope and contents of the prior art.
    2.   Ascertaining the differences between the prior art and the claims at issue.
    3.   Resolving the level of ordinary skill in the pertinent art.
    4.   Considering objective evidence present in the application indicating obviousness
            or nonobviousness.

7.   Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tseng et al.**

(U.S. Patent Application 2006/0117274) in view of **Bowen** (U.S. Patent Application

2003/0105620).

7.1   **Tseng et al.** teaches optimization for live event, real-time, 3D object tracking.

Specifically, as per claim 1, **Tseng et al.** teaches a co-simulation system (Page 7, Para 0178),

comprising: -

        a high-level modeling system (HLMS) (Page 4, Para 0121; Page 70, Para 0855: behavior

model; Page 71, Para 0856 and Para 0857);

a boundary-scan interface coupled to the high-level modeling system (Page 37, Para 0468; Page 38, Para 0476; Page 70, Para 0855) and configured to translate HLMS-issued commands to signals generally compliant with a boundary-scan protocol (Page 038, Para 0476);

a re-configurable hardware platform (Page 9, Para 0191, L1-4) coupled to the boundary-scan interface (Page 038, Para 0476);

a translator coupled to the boundary-scan interface, implemented on the re-configurable hardware platform (Page 9, Para 0191, L1-4; Page 038, Para 0476), and configured to translate input signals generally compliant with the boundary-scan protocol to signals compliant with a second protocol (Page 60, Para 0712, L8-11); and

a first component is configured to transfer input signals of the second protocol to the first component (Page 60, Para 0712, L8-11).

Tseng et al. does not expressly teach a first component instantiated within a wrapper component, wherein the wrapper component is coupled to the translator. **Bowen** teaches a first component instantiated within a wrapper component, wherein the wrapper component is coupled to the translator (Page 28, Para 1183 and Para 1188; Page 29, Para 1244). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Tseng et al.** with the method of **Bowen** that included a first component instantiated within a wrapper component, wherein the wrapper component is coupled to the translator, because that would allow connecting the HDL entry port to the high level model simulator (Page 28, Para 1183).

7.2   As per claim 2, **Tseng et al.** and **Bowen** teach the method of claim 1. **Tseng et al.** and

Rowe et al. do not expressly teach that the wrapper component further includes a memory map.

Bowen teaches that the wrapper component further includes a memory map (Page 28, Para 1183

and Para 1188; Page 29, Para 1244).

        Per claim 3: **Tseng et al.** teaches that the memory map includes a first set of registers for

data input to the first component and a second set of registers for data output from the second

component (Page 11, Para 0208, L5-10; Page 91, Table H).

8.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tseng et al.** (U.S.

Patent Application 2006/0117274) in view of **Bowen** (U.S. Patent Application 2003/0105620),

and further in view of **Lin** (U.S. Patent Application 2004/0236556).

8.1   As per claim 4, **Tseng et al.** and **Bowen** teach the method of claim 1. **Tseng et al.**

teaches that the translator includes a shift register, input data is shifted into the register and output

in parallel to the first component, and output data is input in parallel in the shift register and

shifted out (Page 60, Para 0712, L8-11).

        Tseng et al. and **Bowen** do not expressly teach that the input data is serially shifted and

output data is serially shifted out. **Lin** teaches that the input data is serially shifted and output

data is serially shifted out (Page 14, Para 0170, L2-13). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to modify the method of **Tseng et al.**

and **Bowen** with the method of **Lin** that included the input data being serially shifted and output

data being serially shifted out, because that would allow dynamically allocating multiple

resources to multiple hosts (Page 1, Para 0010, L2-3).

9.   Claims 5-7, 9-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Tseng et al. (U.S. Patent Application 2006/0117274) in view of **Bowen** (U.S. Patent Application

2003/0105620), and further in view of **Chelcea et al.** (U.S. Patent 6,850,092).

9.1   As per claim 5, **Tseng et al.** teaches a system for interfacing a high-level modeling

system (HLMS) with a hardware platform for co-simulation of a first component on the hardware

platform (Page 7, Para 0178; Page 4, Para 0121; Page 70, Para 0855: behavior model; Page 71,

Para 0856 and Para 0857), comprising:

        an interface coupled to the HLMS (Page 37, Para 0468; Page 38, Para 0476; Page 70,

Para 0855) and configured to translate HLMS-issued commands to signals generally compliant

with a boundary-scan protocol (Page 038, Para 0476), and translate signals generally compliant

with a boundary-scan protocol to data compatible with the HLMS (Page 038, Para 0476);

        a translator coupled to the interface, implemented for configuration of the hardware

platform (Page 9, Para 0191, L1-4; Page 038, Para 0476), and configured to translate input signals

generally compliant with the boundary-scan protocol to signals compliant with a second protocol

(Page 60, Para 0712, L8-11); and

        a wrapper component configured to transfer input signals of the second protocol to the first

component (Page 60, Para 0712, L8-11).

Tseng et al. does not expressly teach a translator coupled to the interface, to translate

output signals compliant with the second protocol to signals generally compliant with the

boundary-scan protocol; and transfer output signals of the second protocol to the translator.

Chelcea et al. teaches a translator coupled to the interface, to translate output signals compliant

with the second protocol to signals generally compliant with the boundary-scan protocol; and

transfer output signals of the second protocol to the translator (CL2, L44-65). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

system of **Tseng et al.** with the system of **Chelcea et al.** that included a translator coupled to the

interface, to translate output signals compliant with the second protocol to signals generally

compliant with the boundary-scan protocol; and transfer output signals of the second protocol to

the translator, because that would allow a FIFI circuit having a low latency and high throughput

and capable of operation in mixed environments (CL2, L20-23).

Tseng et al. and Chelcea et al. do not expressly teach a wrapper component implemented

for configuration of the hardware platform, the wrapper component coupled to the translator and

being configured for instantiation of the first component within the wrapper component. **Bowen**

teaches a wrapper component implemented for configuration of the hardware platform, the wrapper

component coupled to the translator and being configured for instantiation of the first component

within the wrapper component (Page 28, Para 1183 and Para 1188; Page 29, Para 1244).

9.2   As per claim 6, **Tseng et al., Bowen** and **Chelcea et al.** teach the system of claim 5.

Tseng et al. teaches memory map circuit coupled to an address decoder circuit (Page 6, Para 0165).

Tseng et al. and **Chelcea et al.** do not expressly teach the wrapper component. **Bowen** teaches the wrapper component (Page 28, Para 1183 and Para 1188; Page 29, Para 1244).

Per claim 7: **Tseng et al.** teaches that the memory map includes a first set of registers for data input to the first component and a second set of registers for data output from the second component (Page 11, Para 0208, L5-10; Page 91, Table H).

9.3   As per claim 9, **Tseng et al.** teaches a method for interfacing a high-level modeling system (HLMS) with a reconfigurable hardware platform for co-simulation of a first component on the reconfigurable hardware platform (Page 7, Para 0178; Page 4, Para 0121; Page 70, Para 0855: behavior model; Page 71, Para 0856 and Para 0857), comprising:

coupling an interface to the HLMS (Page 37, Para 0468; Page 38, Para 0476; Page 70, Para 0855) wherein the interface is configured to translate signals generally compliant. with a boundary-scan protocol to data compatible with the HLMS (Page 038, Para 0476);

configuring the reconfigurable hardware platform with a translator (Page 9, Para 0191, L1-4; Page 038, Para 0476);

coupling the translator to the interface (Page 9, Para 0191, L1-4; Page 038, Para 0476).

Tseng et al. does not expressly teach that the translator is configured to translate signals compliant with a second protocol to signals generally compliant with the boundary-scan protocol; and configured to transfer signals of the second protocol to the translator. **Chelcea et al.** teaches that the translator is configured to translate signals compliant with a second protocol to signals

generally compliant with the boundary-scan protocol; and configured to transfer signals of the

second protocol to the translator (CL2, L44-65).

Tseng et al. and **Chelcea et al.** do not expressly teach wrapper component coupled to the

translator; wherein the wrapper component is configured for instantiation of the first component

within the wrapper component. **Bowen** teaches wrapper component coupled to the translator;

wherein the wrapper component is configured for instantiation of the first component within the

wrapper component (Page 28, Para 1183 and Para 1188; Page 29, Para 1244).

Per claim 10: **Tseng et al.** teaches mapping data input to the first component and data output

from the first component to an addressable memory space (Page 6, Para 0165).

Per claim 11: **Tseng et al.** teaches that the addressable memory space includes a first set of

registers for data input to the first component and a second set of registers for data output from the

second component (Page 11, Para 0208, L5-10; Page 91, Table H).

9.4   As per claim 13, **Tseng et al.** teaches an apparatus for interfacing a high-level modeling

system (HLMS) with a reconfigurable hardware platform for co-simulation of a first component on

the reconfigurable hardware platform (Page 7, Para 0178; Page 4, Para 0121; Page 70, Para

0855: behavior model; Page 71, Para 0856 and Para 0857), comprising:

means for coupling a boundary-scan interface to the HLMS (Page 37, Para 0468; Page

38, Para 0476; Page 70, Para 0855) wherein the boundary-scan interface is configured to translate

HLMS-issued commands to signals generally compliant with a boundary-scan protocol, and

translate signals generally compliant with a boundary-scan protocol to data compatible with the

HLMS (Page 038, Para 0476);

means for configuring the reconfigurable hardware platform with a translator (Page 9, Para

0191, L1-4; Page 038, Para 0476);

means for coupling the translator to the boundary-scan interface (Page 9, Para 0191, L1-4;

Page 038, Para 0476) , wherein the translator is configured to translate input signals generally

compliant with the boundary-scan protocol to signals compliant with a second protocol (Page 60,

Para 0712, L8-11);

and means for transferring input signals of the second protocol to the first component

(Page 60, Para 0712, L8-11).

Tseng et al. does not expressly teach the translator is configured to translate output signals

compliant with the second protocol to signals generally compliant with the boundary-scan

protocol; and for transferring output signals of the second protocol to the translator. **Chelcea et al.**

teaches the translator is configured to translate output signals compliant with the second protocol to

signals generally compliant with the boundary-scan protocol; and for transferring output signals of

the second protocol to the translator (CL2, L44-65).

Tseng et al. and **Chelcea et al.** do not expressly teach means for configuring the wrapper

component to instantiate the first component within the wrapper component. **Bowen** teaches means

for configuring the wrapper component to instantiate the first component within the wrapper

component (Page 28, Para 1183 and Para 1188; Page 29, Para 1244).

10.   Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tseng et al.** (U.S. Patent Application 2006/0117274) in view of **Bowen** (U.S. Patent Application 2003/0105620), and further in view of **Chelcea et al.** (U.S. Patent 6,850,092) and **Lin** (U.S. Patent Application 2004/0236556).

10.1   As per claim 8, **Tseng et al., Bowen** and **Chelcea et al.** teach the system of claim 5. **Tseng et al.** teaches that the translator includes a shift register, input data is shifted into the register and output in parallel to the first component, and output data is input in parallel in the shift register and shifted out (Page 60, Para 0712, L8-11).

        Tseng et al., Bowen and **Chelcea et al.** do not expressly teach that the input data is serially shifted and output data is serially shifted out. **Lin** teaches that the input data is serially shifted and output data is serially shifted out (Page 14, Para 0170, L2-13).

10.2   As per claim 12, **Tseng et al., Bowen** and **Chelcea et al.** teach the method of claim 9. **Tseng et al.** teaches shifting input data into a register and outputting in parallel data from the register to the first component, and storing output data from the first component in parallel in the register and shifting output data from the register to the boundary scan interface (Page 60, Para 0712, L8-11).

        Tseng et al., Bowen and **Chelcea et al.** do not expressly teach serially shifting input data into a register and serially shifting output data from the register. **Lin** teaches serially shifting

input data into a register and serially shifting output data from the register (Page 14, Para 0170, L2-13).

Conclusion

11.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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you have questions on access to the Private PAIR system, contact the Electronic

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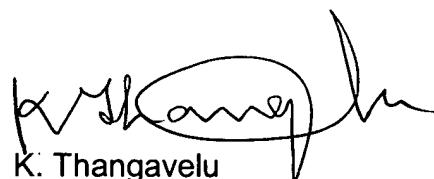
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